

CLAIMS

What is claimed is:

- 1 1. An apparatus, comprising:
2 a phase controller to generate interrelated control signals based upon a
3 comparison of a recovered clock signal with a data signal; and
4 a phase interpolator coupled with said phase controller to change a phase
5 of the recovered clock signal with an analog transition based upon
6 a combination of amplitude contributions from more than one
7 phase of a reference clock signal, wherein the amplitude
8 contributions from the more than one phase are weighted in
9 accordance with the interrelated control signals.
- 1 2. The apparatus of claim 1, further comprising a phase-frequency detector coupled
2 with said phase controller to sample data of the data signal at a sample rate based
3 on the recovered clock signal and to output a comparison signal based on samples
4 of the data.
- 1 3. The apparatus of claim 2, wherein the phase-frequency detector comprises
2 circuitry to compare at least a pre-data bit sample, a mid-data bit sample, and a
3 post-data bit sample to determine the comparison signal.
- 1 4. The apparatus of claim 2, wherein the phase-frequency detector comprises
2 circuitry to modify a phase update rate based upon past phase updates over a
3 period of time in an absence of phase updates.
- 1 5. The apparatus of claim 2, further comprising phase update logic circuitry coupled
2 with the phase-frequency detector to generate charge and discharge signals based
3 upon the comparison signal.
- 1 6. The apparatus of claim 5, wherein the phase update logic circuitry comprises
2 circuitry to manage the distribution of phase updates to a phase control circuit of

3 said phase controller, associated with a managing interrelated control signal of the
4 interrelated control signals.

1 7. The apparatus of claim 1, further comprising a reference clock coupled to said
2 phase interpolator to output more than two phases of the reference clock signal.

1 8. The apparatus of claim 1, wherein said phase controller comprises more than one
2 phase control circuit to generate voltage signals as the interrelated control signals.

1 9. The apparatus of claim 1, wherein said phase controller comprises a first phase
2 control circuit to generate a first interrelated control signal of the interrelated
3 control signals and a second phase control circuit to generate a second interrelated
4 control signal of the interrelated control signals, wherein the second interrelated
5 control signal decreases in amplitude at substantially the same rate as the first
6 interrelated control signal increases in amplitude.

1 10. The apparatus of claim 9, wherein said phase controller further comprises:
2 charge circuitry to transition the amplitude of the first interrelated control
3 signal higher in response to a charge signal; and
4 discharge circuitry to transition the amplitude of the second interrelated
5 control signal lower in response to a discharge signal.

1 11. The apparatus of claim 10, wherein said phase controller further comprises:
2 trip high circuitry to compare the amplitude of the first interrelated control
3 signal to a high amplitude reference; and
4 trip low circuitry to compare the amplitude of the second interrelated
5 control signal to a low amplitude reference.

1 12. The apparatus of claim 1, wherein said phase controller comprises hysteresis
2 circuitry to prevent chatter in an overflow signal.

1 13. The apparatus of claim 1, wherein said phase controller further comprises
2 common mode feedback circuitry coupled with more than one phase control
3 circuit to substantially compensate for changes in a common mode amplitude of
4 managing interrelated control signals of the interrelated control signals.

1 14. The apparatus of claim 1, wherein said phase interpolator comprises phase control
2 circuitry to transition the bias current, based upon the interrelated control signals,
3 of a differential current-steering mechanism to adjust the amplitude contributions.

1 15. The apparatus of claim 14, wherein said phase interpolator comprises a
2 degenerative mesh coupled with the phase control circuitry to degenerate a
3 transfer characteristic of the phase control circuitry.

1 16. The apparatus of claim 15, wherein said phase interpolator further comprises
2 circuitry to filter an output of the differential current-steering mechanism.

1 17. A method, comprising:
2 receiving a data signal;
3 comparing the data signal to a recovered clock signal;
4 generating interrelated control signals based on said comparing; and
5 combining amplitude contributions from phases of a reference clock signal
6 wherein the amplitude contributions are based on the interrelated
7 control signals, to change a phase of the recovered clock signal
8 with an analog transition.

1 18. The method of claim 17, further comprising generating a charge and discharge
2 signal based upon said comparing.

1 19. The method of claim 18, wherein generating a charge and discharge signal
2 comprises generating a charge signal to increase an amplitude of a first
3 interrelated control signal of the interrelated control signals substantially
4 simultaneously with generating a discharge signal to decrease an amplitude of a
5 second interrelated control signal of the interrelated control signals.

1 20. The method of claim 17, further comprising determining an update pattern to
2 provide phase updates for said generating interrelated control signals in the
3 absence of data transitions.

1 21. The method of claim 17, wherein said generating interrelated control signals
2 comprises generating a first control signal and a second control signal to adjust the
3 amplitude contributions from a first phase and a second phase of the phases of the
4 reference clock signal, wherein adjustments to the amplitude contributions of the
5 first phase and the second phase are substantially inversely proportional.

1 22. The method of claim 17, wherein said generating interrelated control signals
2 comprises generating a first ramping control signal and a second ramping control
3 signal, wherein an amplitude of the first ramping control signal increases at a rate

4 substantially equivalent to a rate that an amplitude of the second ramping control
5 signal decreases.

1 23. The method of claim 17, wherein said combining comprises:
2 generating differential signals with at least one of the phases of the
3 reference clock signal, based upon the interrelated control signals;
4 and
5 filtering the differential signals to change the phase of the recovered clock
6 signal with the analog transition.

1 24. The method of claim 23, wherein filtering comprises integrating the differential
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1 25. A system, comprising:
2 a front-end receiver to amplify a data signal;
3 a phase-frequency detector coupled with said front-end receiver to sample
4 data from the data signal based upon a recovered clock signal and
5 generate a comparison signal based on the sampled data;
6 phase update logic circuitry coupled with said phase-frequency detector to
7 generate a signal based upon the comparison signal, to update
8 interrelated control signals;
9 a phase controller coupled with said phase update logic circuitry to
10 generate interrelated control signals based upon the signal; and
11 a phase interpolator coupled with said phase controller to change a phase
12 of the recovered clock signal with an analog transition based upon
13 a combination of amplitude contributions from more than one
14 phase of a reference clock signal, wherein the amplitude
15 contributions from the more than one phase are weighted in
16 accordance with the interrelated control signals.

1 26. The system of claim 25, wherein said phase controller comprises a first phase
2 control circuit to generate a first interrelated control signal of the interrelated
3 control signals and a second phase control circuit to generate a second interrelated
4 control signal of the interrelated control signals, wherein the second interrelated
5 control signal decreases in amplitude at substantially the same rate as the first
6 interrelated control signal increases in amplitude.

1 27. The system of claim 25, wherein said phase interpolator comprises phase control
2 circuitry to transition the bias current of a differential current-steering mechanism
3 based upon the interrelated control signals.

1 28. A machine-readable medium containing instructions, which when executed by a
2 machine, cause said machine to perform operations, comprising:
3 receiving a data signal;
4 comparing the data signal to a recovered clock signal;
5 generating interrelated control signals based on said comparing; and
6 combining amplitude contributions from phases of a reference clock signal
7 wherein the amplitude contributions are based on the interrelated
8 control signals, to change a phase of the recovered clock signal
9 with an analog transition.

1 29. The machine-readable medium of claim 28, wherein said generating interrelated
2 control signals comprises generating a first ramping control signal and a second
3 ramping control signal, wherein an amplitude of the first ramping control signal
4 increases at a rate substantially equivalent to a rate that an amplitude of the second
5 ramping control signal decreases.

1 30. The machine-readable medium of claim 28, wherein said combining comprises:
2 generating differential signals with at least one of the phases of the
3 reference clock signal, based upon the interrelated control signals;
4 and
5 filtering the differential signals to change the phase of the recovered clock
6 signal with the analog transition.